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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/609,158	06/27/2003	Nathan Laredo	TRAN-P206	7870
7590	01/07/2008		EXAMINER	
WAGNER, MURABITO & HAO LLP Two North Market Street, Third Floor San Jose, CA 95113			TANG, KENNETH	
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	10/609,158	LAREDO ET AL.
	Examiner	Art Unit
	Kenneth Tang	2195

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 16 October 2007.  
 2a) This action is FINAL.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-30 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-30 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | Paper No(s)/Mail Date: _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application |
|  | 6) <input type="checkbox"/> Other: _____                          |

## DETAILED ACTION

1. This action is in response to the Amendment on 10/16/07. Applicant's arguments have been fully considered but they are considered moot in view of the new grounds of rejections.
2. Claims 31-32 have been cancelled by the Applicant. Claims 1-30 are now presented for examination.

### *Claim Rejections - 35 USC § 101*

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. The computer readable media of claims 21-30 are directed to non-statutory subject matter.
4. In claim 21, it is directed to a computer readable media that may allude to a signal, as shown in the Applicant's Specification (page 5, lines 4-8). In the case where the computer readable media relate to signals, the claim fails to comply with any of the four statutory categories, and therefore, it is non-statutory under 35 USC 101. 35 U.S.C. 101 defines four categories of inventions that Congress deemed to be the appropriate subject matter of a patent: processes, machines, manufactures and compositions of matter. The latter three categories define "things" or "products" while the first category defines "actions" (i.e., inventions that consist of a series of steps or acts to be performed). See 35 U.S.C. 100(b) ("The term process' means process, art, or method, and includes a new use of a known process, machine, manufacture, composition of matter, or material.").

5. Applicant's amendment to the Specification on 10/16/07 is not sufficient to overcome the 35 USC § 101 rejection because the Applicant's amendment does not have the electrical or magnetic signals excluded from the claimed computer readable media. The Examiner recommends defining, in the Specification, a "transmission media" that relates to the electrical or magnetic signals and a separate "computer readable storage media" (and amending the computer readable media to be a "computer readable storage media" in the claim language for consistency) that stores computer readable code.

6. Claims 22-30 are also rejected as claims dependent upon rejected claim 21.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. **Claims 1-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Devine et al. (hereinafter Devine) (US 6,397,242 B1) in view of Patel et al. (hereinafter Patel) (US 2004/0215444 A1).**

8. As to claim 1, Devine teaches a method for supporting input/output for a virtual machine (see Fig. 1-2), comprising:

executing virtual machine application instructions, wherein the application instructions are executed using micro architecture code of a processor architecture (col. 2, lines 27-35, col. 9, lines 11-12, etc.);

receiving an I/O access from the virtual machine application (col. 2, lines 21-36, col. 13, lines 20-36, Fig. 1-2);

upon receiving the I/O access, generate an exception (col. 7, lines 6-13, col. 8, lines 40-43);

performing the I/O access by using a host operating system (col. 11, lines 34-40, col. 12, line 50);

updating state data for the virtual machine application in accordance with the I/O access (col. 5, lines 60-67 through col. 6, lines 1-6); and

resuming execution of the virtual machine application (Resume 242, Fig. 2, col. 21, lines 56-60).

9. Devine is silent in the micro architecture code includes an instruction interpreter to execute the virtual machine application instructions.

10. However, Patel discloses using a virtual machine such as a Java Virtual Machine (JVM) and that the Java bytecode interpreter is one component of the JVM (page 1, [0004], lines 7-8).

To execute a Java program, a bytecode interpreter takes the Java bytecodes and converts them to equivalent native processor instructions and executes the Java program (page 1, [0004], lines 4-7).

Devine and Patel are analogous art because they both involve using virtual machines. One of ordinary skill in the art would have known to modify Devine's virtual machine system such that an interpreter would be included to execute the virtual machine application instructions. The

suggestion/motivation for doing so would have been to provide the predicted result of translation of instructions in a platform independent environment (page 1, [0003], [0005]). Therefore, it would have been obvious to combine Devine and Patel to obtain the invention of claim 1.

11. As to claim 2, Patel teaches wherein the micro architecture code includes an instruction interpreter is further configured to function with an instruction translator to translate target instructions into host VLIW instructions to execute the virtual machine application instructions (page 3, [0029], lines 3-9).

12. As to claim 3, Devine (Fig. 2, 230) and Patel (translator unit) (page 3, [0029], line 7) teaches wherein the micro architecture code includes an instruction translator to execute the virtual machine application instructions (Fig. 2, 230).

13. As to claim 4, Devine teaches further comprising:  
executing a monitor to implement the I/O access from the virtual machine application,  
wherein the monitor is configured to handle the exception caused by the I/O access (virtual  
machine monitor, see Abstract, col. 5, lines 13-30).

14. As to claim 5, Devine teaches further comprising:  
entering the single step mode, wherein the monitor single steps through the application  
instructions to handle the exception (col. 11, lines 34-48, col. 12, lines 49-52).

15. As to claim 6, Devine teaches further comprising:

using the monitor to maintain at least one virtual device to implement the I/O access from the virtual machine application (col. 24, lines 63-67).

16. As to claim 7, Devine teaches further comprising:

using the host operating system to access a real device in response to an access to the virtual device (Fig. 7, 700, 720, 750, 710, 100, col. 24, lines 60-67, etc.); and updating the state data for the virtual machine application in accordance with I/O data retrieved from the real device (col. 5, lines 60-67 through col. 6, lines 1-6).

17. As to claim 8, Devine (see Fig. 1, col. 2, lines 27-35, col. 9, lines 11-12) and Patel (page 3, [0029], lines 3-9) teach wherein the virtual machine application instructions comprise target instructions and the micro architecture code comprises host instructions.

18. As to claim 9, Devine (col. 2, line 32) and Patel (page 3, [0029], lines 3-9) teaches wherein the target instructions are x86 instructions and the host instructions are VLIW instructions.

19. As to claim 10, Devine teaches wherein the virtual machine is an x86 compatible virtual machine (col. 9, lines 7-11).

20. As to claim 11, Devine teaches a system for supporting input/output for a virtual machine (Fig. 1-2), comprising:

a processor architecture including micro architecture code configured to execute, natively on a CPU hardware unit of the processor architecture (col. 2, lines 27-35, col. 9, lines 11-12);  
and

a memory coupled to the processor architecture, the memory storing virtual machine application instructions, wherein the application instructions are executed using the micro architecture code, the micro architecture code causing the processor architecture to implement a method comprising (col. 13, lines 20-36):

receiving an I/O access from the virtual machine application (col. 25, lines 14-21, etc.);  
upon receiving the I/O access, generating an exception (col. 25, lines 14-21, etc.);  
performing the I/O access by using a host operating system (Fig. 7, 700, 720, 750, 710, 100, etc.);

updating state data for the virtual machine application in accordance with the I/O access (col. 5, lines 60-67 through col. 6, lines 1-6); and

resuming execution of the virtual machine application (Resume 242, Fig. 2, col. 21, lines 56-60).

21. Devine is silent in the micro architecture code includes an instruction interpreter to execute the virtual machine application instructions.

22. However, Patel discloses using a virtual machine such as a Java Virtual Machine (JVM) and that the Java bytecode interpreter is one component of the JVM (page 1, [0004], lines 7-8). To execute a Java program, a bytecode interpreter takes the Java bytecodes and converts them to

equivalent native processor instructions and executes the Java program (page 1, [0004], lines 4-7). Devine and Patel are analogous art because they both involve using virtual machines. One of ordinary skill in the art would have known to modify Devine's virtual machine system such that an interpreter would be included to execute the virtual machine application instructions. The suggestion/motivation for doing so would have been to provide the predicted result of translation of instructions in a platform independent environment (page 1, [0003], [0005]). Therefore, it would have been obvious to combine Devine and Patel to obtain the invention of claim 1.

23. As to claims 12-21, they are rejected for the same reasons as stated in the rejections of claims 2-11.

24. As to claims 22-30, they are rejected for the same reasons as stated in the rejections of claims 2-10.

*Response to Arguments*

**25. Applicant argues that the 35 USC § 101 should be withdrawn in view of the Amendment to the Specification on 10/16/07.**

26. In response, the Applicant's amendment to the Specification on 10/16/07 is not sufficient to overcome the 35 USC § 101 rejection because the Applicant's amendment does not have the electrical or magnetic signals excluded from the claimed computer readable media. Therefore the rejection regarding 35 USC § 101 is not withdrawn. The Examiner recommends defining, in

the Specification, a “transmission media” that relates to the electrical or magnetic signals and a separate “computer readable storage media” (and amending the computer readable media to be a “computer readable storage media” in the claim language for consistency) that stores computer readable code.

27. Applicant’s amendment has overcome the rejections of 35 USC § 112, and therefore, the Examiner has withdrawn these rejections.

28. **Applicant argues regarding claims 2, 12, and 22 that the prior art does not teach the amended claim limitations.**

29. Patel teaches wherein the micro architecture code includes an instruction interpreter is further configured to function with an instruction translator to translate target instructions into host VLIW instructions to execute the virtual machine application instructions (page 3, [0029], lines 3-9).

30. **Applicant argues regarding claims 3, 13, and 23, that there is no disclosure of translation (e.g., from a host instruction set to a target instruction set) to run both the virtual machine monitor and the virtual machine.**

In response, Devine's virtual machine monitor is equivalent to a translator. This is shown in Devine's abstract as it discloses that the VMM includes a binary translation subsystem (see Abstract, lines 6-8). Furthermore, Patel discloses using a virtual machine such as a Java Virtual Machine (JVM) and that the Java bytecode interpreter is one component of the JVM (page 1,

[0004], lines 7-8). To execute a Java program, a bytecode interpreter takes the Java bytecodes and converts them to equivalent native processor instructions and executes the Java program (page 1, [0004], lines 4-7). In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., translation from a host instruction set to a target instruction set) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

**31. Applicant argues regarding claims 8, 18, and 28, that Devine does not teach the application instructions comprise target instructions and the micro architecture code comprises host instructions.**

32. In response, Devine teaches binary translation (see Abstract, lines 6-8). In addition, Patel teaches translating to VLIW instructions as one example (page 3, [0029], lines 3-9).

33. Applicant does not present any arguments for claims 4-7, 9-10, 14-17, 19-20, 24-27, and 29-30.

### ***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- Bala et al. (US 2002/0184618 A1) discloses a virtual machine using an interpreter to translate x86 instruction sets to/from a VLIW instruction set (see paragraph [0073]).
- O'Connor et al. (US 6,961,843 B2) discloses a virtual machine that translates instructions to a VLIW processor (col. 3, lines 44-64).

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth Tang whose telephone number is (571) 272-3772. The examiner can normally be reached on 8:30AM - 6:00PM, Every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Kt  
1/1/08



MENG-AL T. AN  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2100